Spécialité de Master « Optique, Matière, Paris »

Stage de recherche (4 mois minimum, à partir de début mars)

Proposition de stage (ne pas dépasser 1 page)

Date de la proposition : 15/11/2017

Responsable du stage / *internship supervisor*:

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Nom du Laboratoire / *laboratory name*:

Code d'identification :UMR 8630 Organisme : Observatoire de Paris / CNRS / UPMC
Site Internet / *web site*: http://syrte.obspm.fr/tfc/frequences_optiques/accueil.php
Adresse / *address: 77 avenue Denfert Rochereau 75014 Paris*
Lieu du stage / *internship place*: Observatoire de Paris + CNAM (rue Saint Martin Paris)

Titre du stage / *internship title*: FPGA-based all numerical phase lock loop for phase-slip-free optical timescales

Résumé / *summary*

Optical frequency standard are planned to become the base of the new redifinition of the SI second in the next 10 years. A timescale based on optical frequency standards will involve many lasers whose optical phase needs to be precisely controlled and maintained over the course of months and years without cuycle-slips of temporary loss of coherence. Currently used analog-electronics based techniques exhibits fast feed-back bandwidth and low-noise. They are however not sufficiently reliable and even in the best conditions may exhibit a few cycle-slips par months. This is particularly detremental to the development and dissemination of purely optical timescales which will be a cornerstone of the future SI optical second implementation.

A possibility to solve this issue is to realize purely digital phase-lock loops, where the phase of the beatnote between two lasers is continuously tracked and servo-ed with a practically infinite dynamics (whereas analog systems are limited to typically 2pi). Since this full digital phase-lock loop still needs reasonnably large feedback bandwidth (~1MHz), the FPGA platform seems to be the hardwaree of choice for such a development.

The internship will be about realizing such an all-digital phase lock loop on a redpitaya system, and test its efficiency and performance on experimental optical beatnotes and real lasers.

The internship will be located partly at CNAM (Paris 3eme) where highly qualified supervision and support for FPGA design develoment is available, and partly at SYRTE (Paris 14eme), where the SYRTE laboratory has a long-dstanding expertise on fast phase lock-loop for lasers and application to high precision measurement.

The internet will need a strong motivation to realize FPGA-design development, electronics hardware developments, opto-electronic tests and characterization.

Although most of the supervision can be done in French, some capability of working in English would be also useful to interact with junior and senior memebers of the SYRTE optical frequency group, which will be hosting this internship.

Ce stage pourra-t-il se prolonger en thèse ? *Possibility of a PhD* **? : oui**

Si oui, financement de thèse envisagé/ *financial support for the PhD***: contrat doctoral / other**

Lumière, Matière, Interactions	**OUI**	Lasers, Optique, Matière	**OUI**